IN THE CLAIMS:

Claims 1 and 2 (Cancelled)

3. (Previously Amended) A semiconductor memory device comprising:

a plurality of input terminals for receiving write data, a control signal and an address signal; and

at least one output terminal, different in number from the input terminal(s) for receiving the write data, for outputting read data, wherein the input terminals are coupled to a first bus, and said at least one output terminal is coupled to a second bus, and each of the first and second buses is a unidirectional bus for transferring a signal or data in one direction.

4. (Previously Amended) A semiconductor memory device comprising:

a plurality of input terminals for receiving write data, a control signal and an address signal;

at least one output terminal, different in number from the input terminal(s) for receiving the write data, for outputting read data,

a write conversion circuit coupled between an internal data bus and the input terminal(s) for converting write data applied to said input terminal(s) into internal write data being equal in bit width to said internal data bus, and outputting said internal write data; and

a read conversion circuit coupled between said internal data bus and the output terminal for converting internal read data read onto said internal data bus into data being

equal in bit width to said at least one output terminal, and transferring converted data to said at least one output terminal.

5. (Original) The semiconductor memory device according to claim 4, wherein

said write conversion circuit includes a serial/parallel conversion circuit for sequentially receiving write data applied to said input terminal(s), and transferring received write data in parallel onto said internal data bus, and

said read conversion circuit includes a parallel/serial conversion circuit for receiving data of a plurality of bits read in parallel onto said internal data bus, and converting said data of a plurality of bits into serial data to sequentially transfer said serial data to said at least one output terminal.

6. (Original) The semiconductor memory device according to claim 5, further comprising a data-bit control circuit for changing a bit width of input data of said serial/parallel conversion circuit and a bit width of output data of said parallel/serial conversion circuit.

7. (Original) The semiconductor memory device according to claim 4, further comprising a data-bit control circuit for changing a number of bits of input data of said write conversion circuit and a number of bits of output data of said read conversion circuit.

8. (Original) The semiconductor memory device according to claim 4, further comprising a control circuit for operating said write conversion circuit and said read conversion circuit in parallel.

9. (Original) A memory system, comprising:

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a memory for storing information;

a memory controller for controlling access to said memory;

a first unidirectional bus for transferring write data, a control signal and an address signal from said memory controller to said memory; and

a second unidirectional bus for transferring read data from said memory to said memory controller, said read data being allowed to be different in bit width from said write data.

10. (Original) The memory system according to claim 9, wherein said memory includes:

a write circuit for receiving said write data to produce internal write data;

a read circuit for producing said read data from internal read data that is read internally; and

a data-bit changing circuit for changing a number of bits of input data of said write circuit and a number of bits of output data of said read circuit.

11. (Original) The memory system according to claim 9, wherein said memory controller includes a circuit for changing a number of bits of said write data and a number of bits of said read data.

12. (Original) The memory system according to claim 9, wherein said memory includes circuitry for simultaneously inputting and outputting said write data and said read data.

13. (Original) The memory system according to claim 9, wherein said memory controller includes circuitry for simultaneously transferring said write data and said read data.

14. (Original) The memory system according to claim 9, wherein said first unidirectional bus transfers the write data, the control signal and the address signal through common data bus lines.

15. (Previously Amended) The semiconductor memory device according to claim 3, wherein the input terminals receive the write data, the control signal and the address signal at common terminals.

16. (Currently Amended) The ~~A~~ semiconductor memory device according to claim 3, wherein said read data is different in bit width from said write data.

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17. (Currently Amended) The ~~A~~ semiconductor memory device according to claim 4, wherein said read data is different in bit width from said write data.